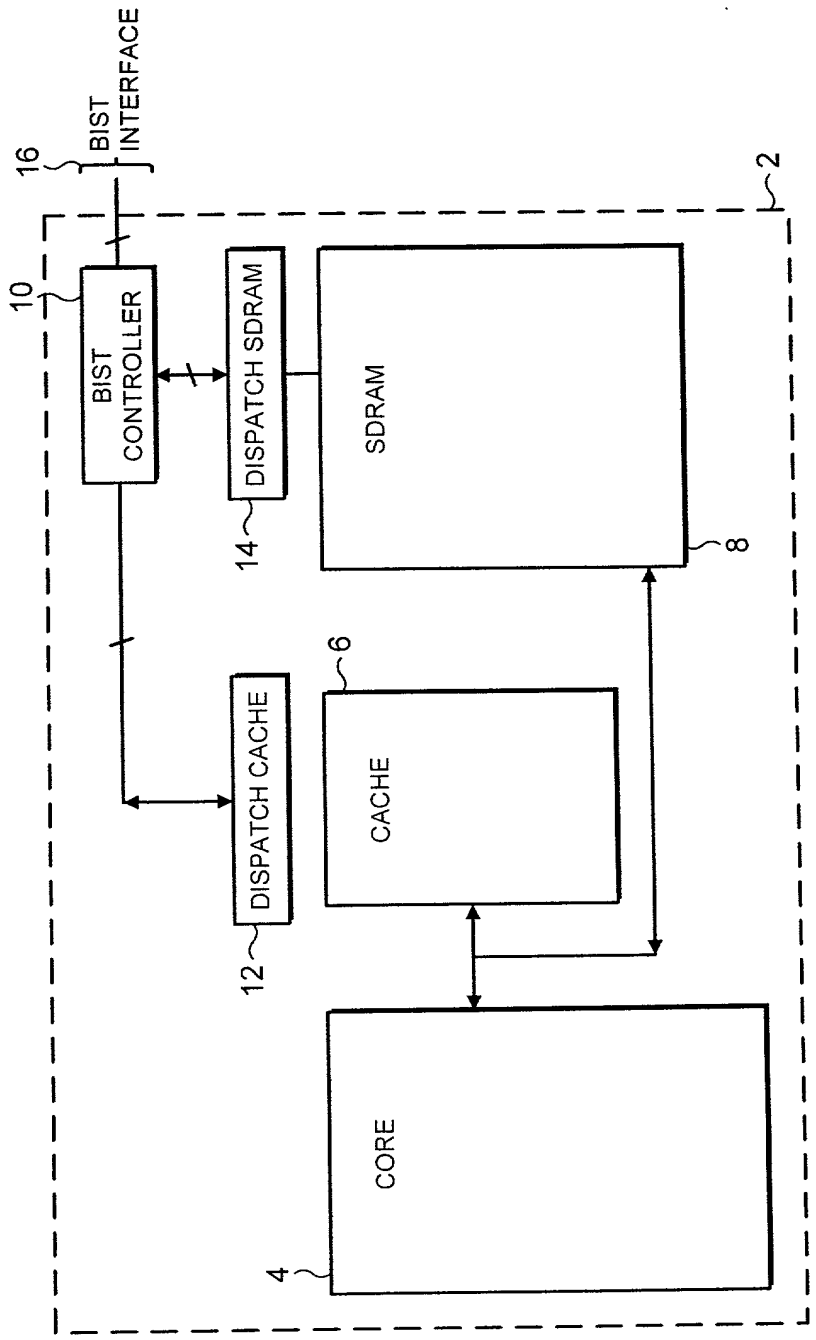
16
BIST INTERFACE
2
10
BIST CONTROLLER
DISPATCH SDRAM
SDRAM
14
8
6
DISPATCH CACHE
CACHE
12
CORE
4

FIG. 1

Applied Materials

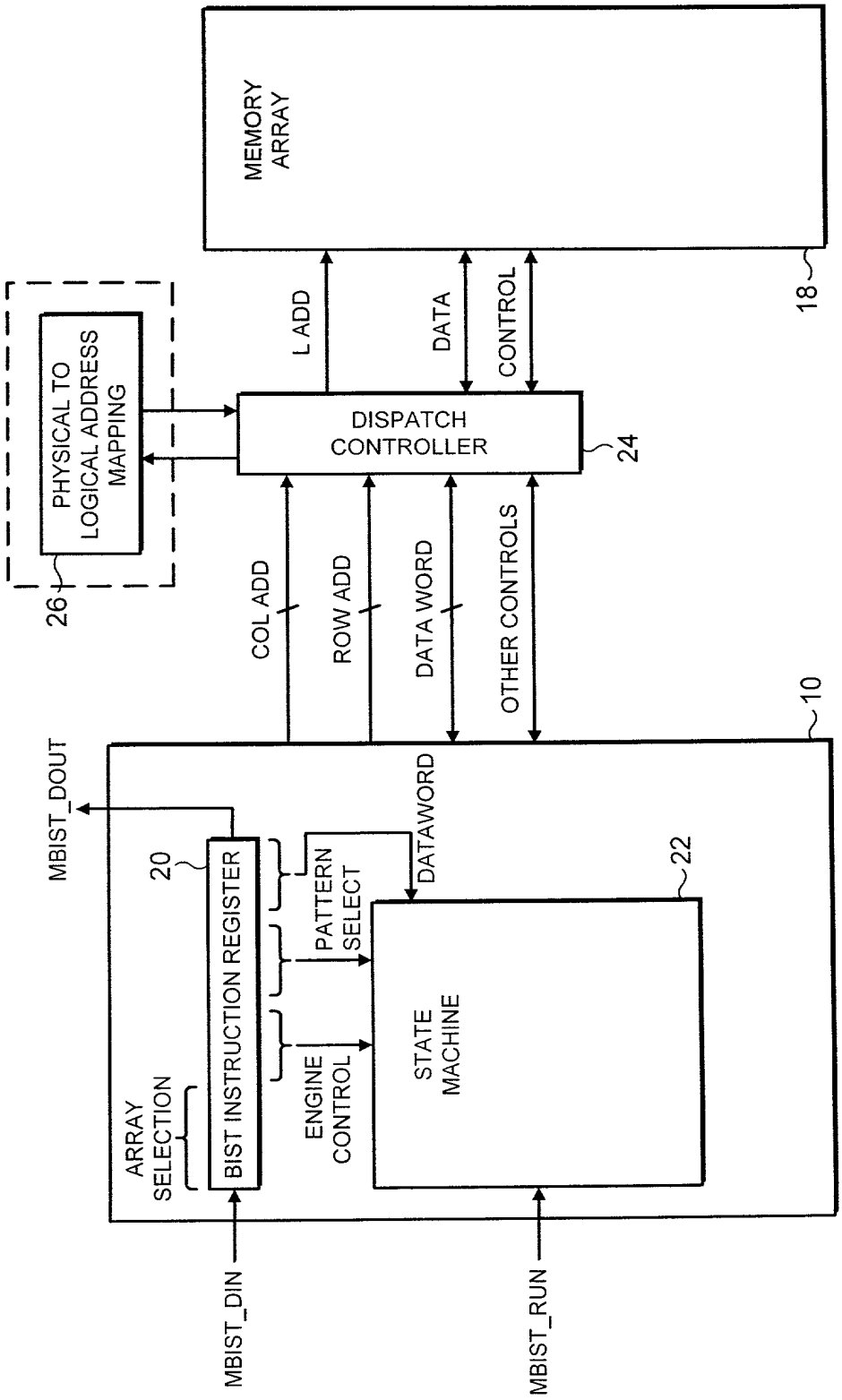

FIG. 2

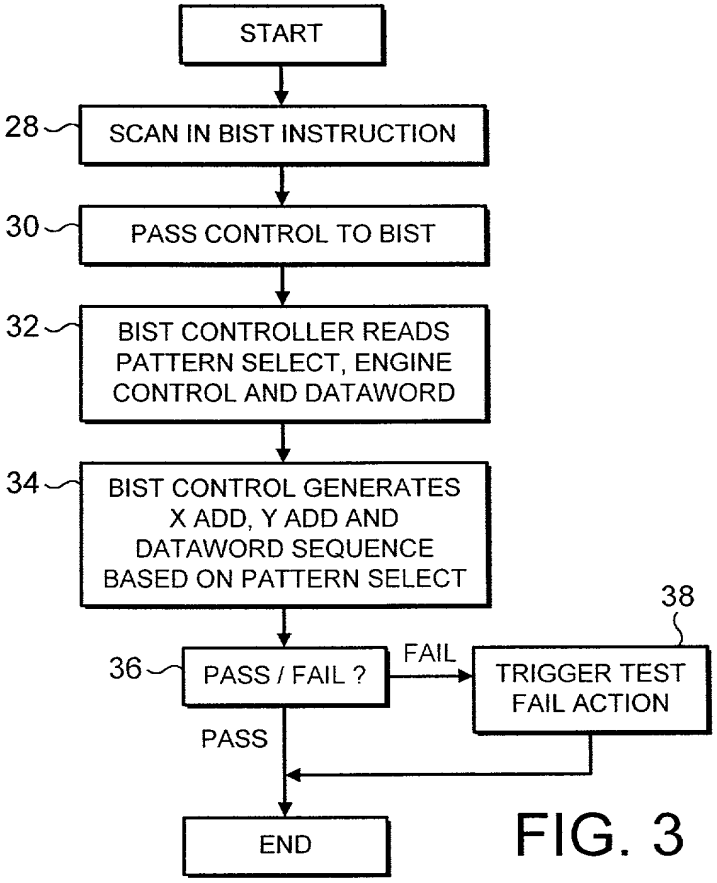
START
28
SCAN IN BIST INSTRUCTION
30
PASS CONTROL TO BIST
32
BIST CONTROLLER READS PATTERN SELECT, ENGINE CONTROL AND DATAWORD
34
BIST CONTROL GENERATES X ADD, Y ADD AND DATAWORD SEQUENCE BASED ON PATTERN SELECT
38
36
PASS / FAIL ?
FAIL
TRIGGER TEST FAIL ACTION
PASS
END

FIG. 3

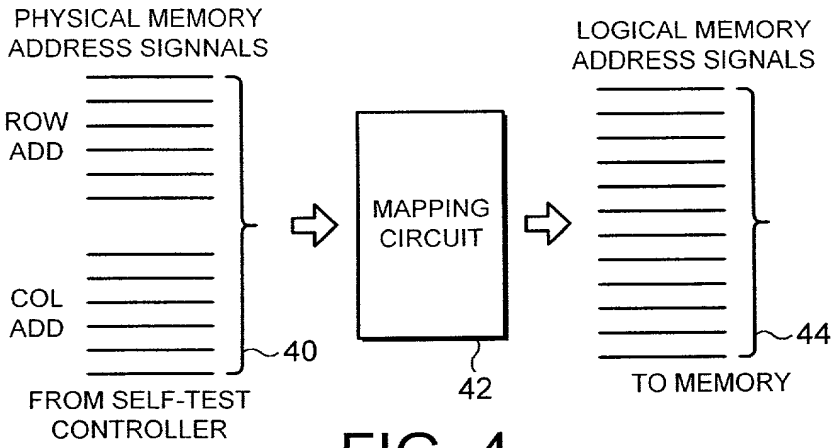
PHYSICAL MEMORY ADDRESS SIGNNALS
ROW ADD
COL ADD
40
FROM SELF-TEST CONTROLLER
MAPPING CIRCUIT
42
LOGICAL MEMORY ADDRESS SIGNALS
44
TO MEMORY

FIG. 4

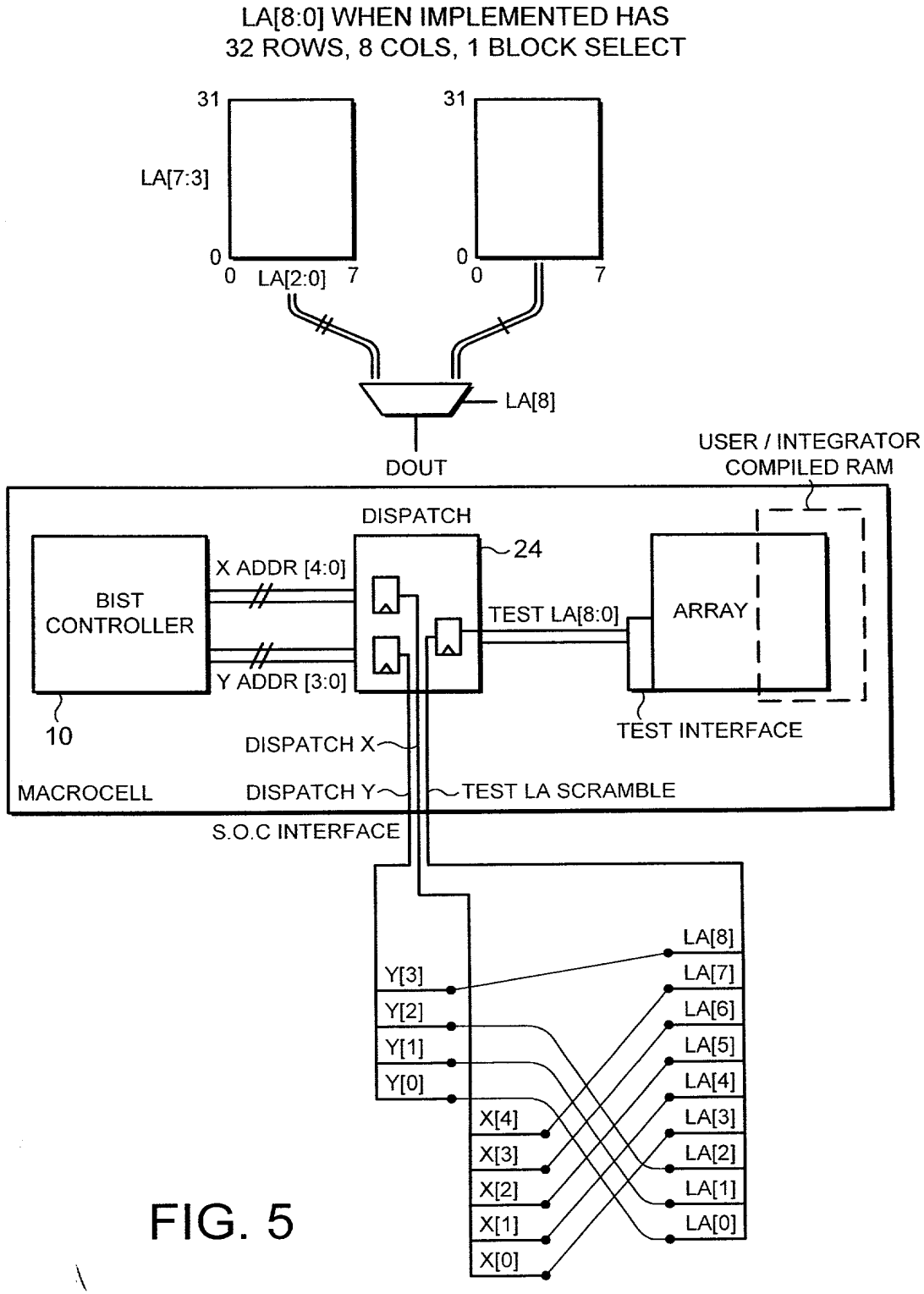
LA[8:0] WHEN IMPLEMENTED HAS
32 ROWS, 8 COLS, 1 BLOCK SELECT
31
LA[7:3]
0
0
LA[2:0]
7
31
0
0
7
LA[8]
DOUT
USER / INTEGRATOR
COMPILED RAM
DISPATCH
24
BIST
CONTROLLER
X ADDR [4:0]
Y ADDR [3:0]
TEST LA[8:0]
ARRAY
10
TEST INTERFACE
DISPATCH X
MACROCELL
DISPATCH Y
TEST LA SCRAMBLE
S.O.C INTERFACE
Y[3]
Y[2]
Y[1]
Y[0]
X[4]
X[3]
X[2]
X[1]
X[0]
LA[8]
LA[7]
LA[6]
LA[5]
LA[4]
LA[3]
LA[2]
LA[1]
LA[0]

FIG. 5